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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,134	09/10/2003	Mohammad R. Mirabedini	03-0730	4827

24319 7590 08/03/2005

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,134	MIRABEDINI ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *10-19* is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 9* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 07/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 10-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on June 29, 2005.

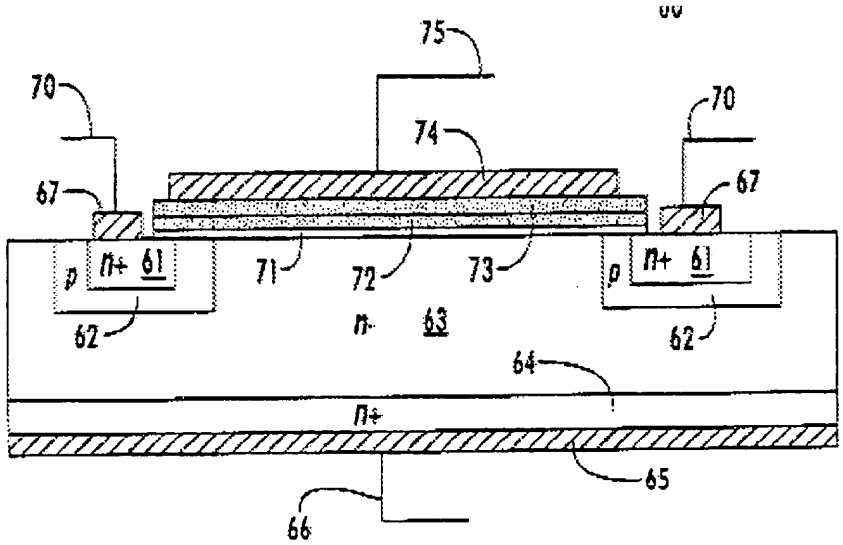
Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, are rejected under 35 U.S.C. 102(b) as being anticipated by Lipkin et al., U.S. Patent 6,437,371 B2.

Lipkin discloses a semiconductor process as claimed. See **FIGS. 1-9**, where Lipkin teaches the following limitations.



4. Pertaining to claim 1, Lipkin teaches a method of forming a portion of an integrated circuit comprising:

providing a silicon carbide base **64**;

epitaxially growing a dielectric film on the silicon carbide base (please note that barium strontium titanate dioxide is a perovskite oxide, meaning that it is single crystal, column 4, line 23 discloses BST oxide); and forming a CMOS device on the silicon carbide base and epitaxially grown dielectric film, wherein the CMOS device includes a channel region and a gate dielectric, the channel region is formed in the silicon carbide base and the gate dielectric is formed by the epitaxially grown dielectric film.

5. Pertaining to claim 2, Lipkin teaches a method as defined in claim 1 wherein:

the step of epitaxially growing the dielectric film further comprises forming a crystalline carbon-containing film **63** on the silicon carbide base **64**.

6. Pertaining to claim 3, Lipkin teaches a method as defined in claim 1 wherein:

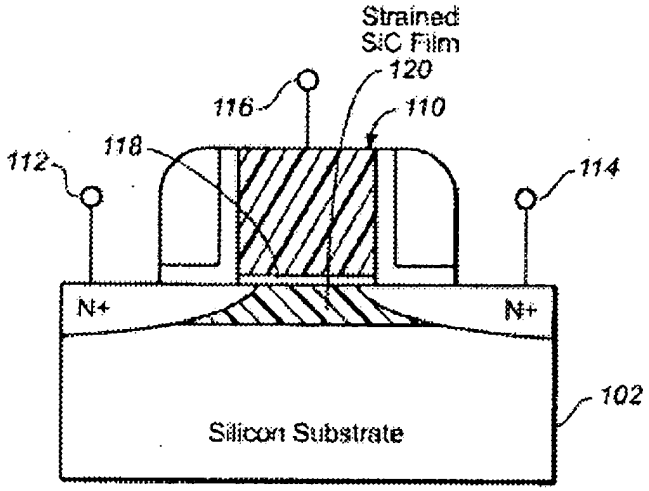
the step of epitaxially growing the dielectric film further comprises forming a crystalline carbon film on the silicon carbide base (see the rejection of claim 2 above). Please note that the Examiner objects to claim 3 as being substantially duplicate of claim 2. Correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lipkin et al., U.S. Patent 6,437,371 B1 in view of Applicants Admitted Prior Art FIG. 2.



9. Pertaining to claim 4, Lipkin fails to teach a method as defined in claim 1 further comprising: providing a silicon substrate;

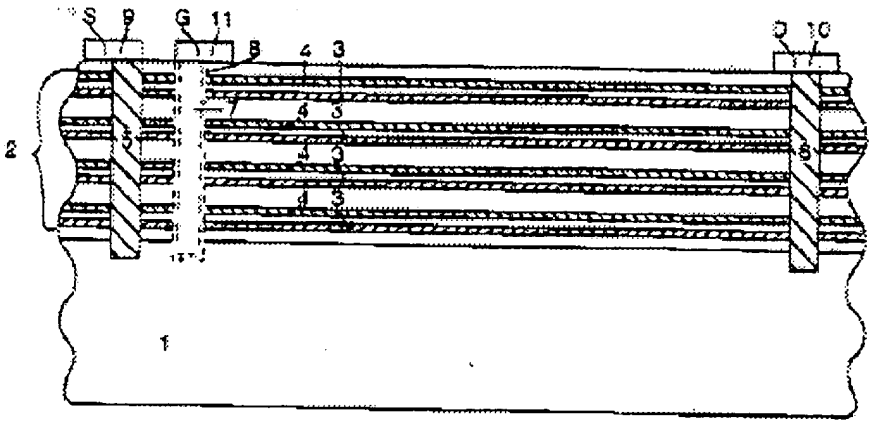
and the step of providing the silicon carbide base further comprises epitaxially growing the silicon carbide base on the silicon substrate. AAPA teaches providing a silicon substrate. In view of AAPA, it would have been obvious to one of ordinary skill in the art to incorporate the silicon substrate of AAPA into the Lipkin semiconductor process because of improved carrier mobility (see pp 4).

10. Claims 5, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipkin et al., U.S. Patent 6,437,371 B1 in view of Tihanyi et al, U.S. Patent 6,365,919 B1.

Lipkin discloses a semiconductor process substantially as claimed.

Pertaining to claim 5, Lipkin fails to teach a method as defined in claim 1 wherein:

the step of forming the CMOS device further comprises forming a silicon carbide region on the epitaxially grown dielectric film, wherein the CMOS device further includes a gate electrode formed by the silicon carbide region. Tihanyi teaches forming a gate electrode comprised of silicon carbide. In view of Tihanyi it would have been obvious to one of ordinary skill to incorporate the silicon carbide gate electrode into the Lipkin semiconductor process because of the possible layout for such a silicon carbide junction field effect transistor (column 3, lines 24-25).



11. Pertaining to claim 6, Lipkin fails to teach a method as defined in claim 5 wherein: the step of forming the silicon carbide region on the epitaxially grown dielectric film further comprises epitaxially growing a silicon carbide layer on the epitaxially grown dielectric film. Tihanyi teaches an epitaxially grown silicon carbide layer. In view of Tihanyi it would have been obvious to one of ordinary skill to incorporate the silicon carbide gate electrode into the Lipkin semiconductor process because of the possible layout for such a silicon carbide junction field effect transistor (column 3, lines 24-25).

12. Pertaining to claim 7, Lipkin fails to teach a method as defined in claim 5 wherein: the step of forming the silicon carbide region on the epitaxially grown dielectric film further comprises depositing a silicon carbide layer on the epitaxially grown dielectric film. In view of Tihanyi it would have been obvious to one of ordinary skill to incorporate the silicon carbide gate electrode into the Lipkin semiconductor process because of the possible layout for such a silicon carbide junction field effect transistor (column 3, lines 24-25).

Allowable Subject Matter

13. Claims 8 and 9 allowed.

14. The following is an examiner's statement of reasons for allowance: the prior art does not anticipate nor render obviousness as to depositing a silicon carbide film on an epitaxially strained silicon carbide film.

15. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC